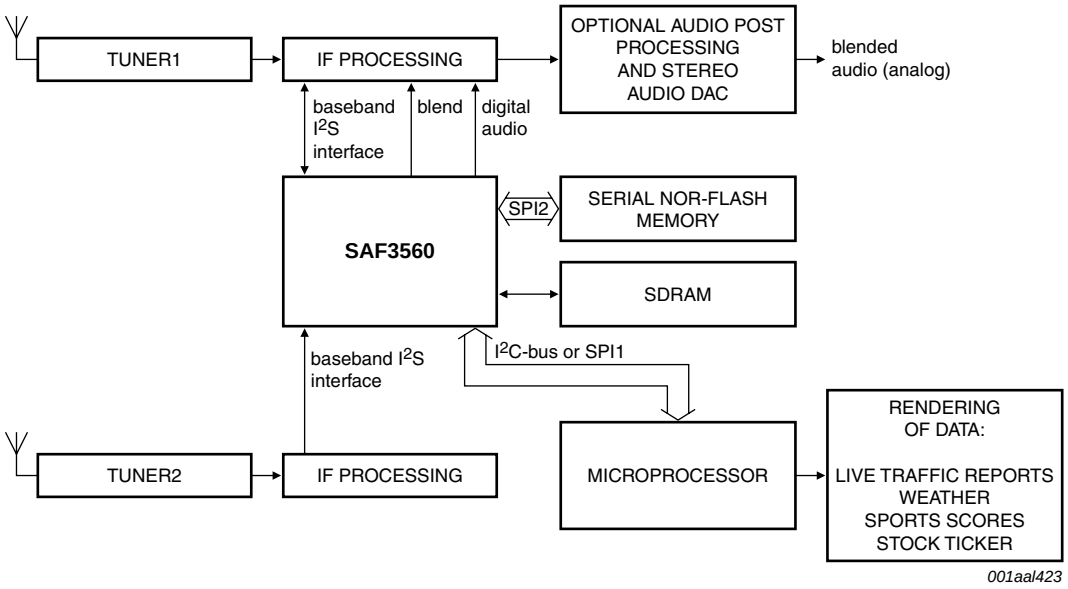
SAF3560

Terrestrial digital radio processor

Rev. 03 — 15 September 2010 **Product short data sheet**

1. General description

The SAF3560 is a digital radio processor that demodulates and processes digital terrestrial baseband signals, such as HD Radio signals, into audio signals and digital data signals.



(1) Second input only supported by specific types (see Table 3)

Fig 1. System block diagram

Major benefits of terrestrial radio processor systems with SAF3560 are:

- Compatibility with conventional baseband radio reception ICs
- Dramatically improved reception and sound quality
- CD-sound quality without noise, interference and multipath fading for FM
- Providing new data services
- HD Radio reception including audio processing
- Voltage partitioning of I/Os

System designers can add digital terrestrial radio capability in a simple and inexpensive way through the SAF3560. The SAF3560 decodes digital radio input to provide digital audio and also processes digital data. Multiple interfaces give flexibility while integrating the SAF3560 into the receiver system.

2. Features and benefits

2.1 HD Radio technology

- HD Radio signal decoding for AM and FM digital audio
- Dual HD Radio support for support of 2nd station for background scanning and data service
- Front-end to baseband interface support through serial baseband I^2S-bus type interface
- Secondary baseband interface for dual tuner applications
- Metadata support for HD Radio reception
- Data services support for HD Radio reception
- Advanced HD Radio feature support, such as[1]:
  - Conditional Access (CA)
  - Store and replay
  - Apple ID3 tag
  - Multicasting
  - Electronic Program Guide (EPG)

2.2 Digital audio

- Up to 6 channel (5.1) audio support through I^2S-bus serial audio interface
- Optional SRC (8 kHz to 48 kHz) for up to 6 channels of I^2S-bus audio output
- I^2S-bus serial audio input for auxiliary processing
- Optional SRC (8 kHz to 48 kHz) for I^2S-bus input
- Optional restricted support for 96 kHz input and output sample-rate conversion
- Optional digital audio output through S/PDIF (without SRC)
- Basic audio processing for external digital audio sources
- Advanced audio processing (please contact NXP for a list of supported audio processing features: Section 14 “Contact information”)

2.3 Memory

- Supports SDR-SDRAM controller (up to 512 Mbit in 16-bit configuration)
- Supports serial NOR-Flash memory with various sizes depending on the actual application

1. Please contact NXP for a detailed list of supported feature sets: Section 14 “Contact information”.

2.4 Other peripheral interfaces

- Two I^2C-bus interfaces
- Three Serial Peripheral Interfaces (SPI)
- One UART interface
- Five individual GPIO pins for applications and diagnostics
- One JTAG interface for diagnostics

2.5 Miscellaneous

- One internal clock oscillator and two internal Phase-Locked Loops (PLL)
- Powerful signal and audio processing core architecture
- Qualified in accordance with *AEC-Q100*

3. Quick reference data

Table 1. Power supply characteristics

After power-up the SAF3560 needs a reset pulse for at least 2 ms.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltages						
$V_{DDA(OSC)(1V2)}$	oscillator analog supply voltage (1.2 V)		1.14	1.2	1.32	V
$V_{DDA(PLL)(1V2)}$	PLL analog supply voltage (1.2 V)		1.14	1.2	1.32	V
$V_{DDD(C)(1V2)}$	core digital supply voltage (1.2 V)		1.14	1.2	1.32	V
$V_{DDD(DAB)(3V3)}$	DAB digital supply voltage (3.3 V)		3.0	3.3	3.6	V
$V_{DDD(DSP)(3V3)}$	DSP digital supply voltage (3.3 V)		3.0	3.3	3.6	V
$V_{DDD(JTAG)(3V3)}$	JTAG digital supply voltage (3.3 V)		3.0	3.3	3.6	V
$V_{DDD(MC)(3V3)}$	microcontroller digital supply voltage (3.3 V)		3.0	3.3	3.6	V
$V_{DDD(MEM)(1V2)}$	memory digital supply voltage (1.2 V)		1.14	1.2	1.32	V
$V_{DDD(SDRAM)(3V3)}$	SDRAM digital supply voltage (3.3 V)		3.0	3.3	3.6	V
Supply currents						
I_{DD}	supply current	all core related blocks [1]	-	90	116	mA
		all I/O related blocks [2]	-	28	37	mA
Power dissipation						
P_{tot}	total power dissipation		-	0.2	0.5	W

[1] Through pins $V_{DDA(OSC)(1V2)}$, $V_{DDA(PLL)(1V2)}$, $V_{DDD(C)(1V2)}$ and $V_{DDD(MEM)(1V2)}$.

[2] Through pins $V_{DDD(DAB)(3V3)}$, $V_{DDD(DSP)(3V3)}$, $V_{DDD(JTAG)(3V3)}$, $V_{DDD(MC)(3V3)}$ and $V_{DDD(SDRAM)(3V3)}$.

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
SAF3560HV/V1100	HLQFP144	plastic thermal enhanced low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm; exposed die pad	SOT612-4
SAF3560HV/V1101	HLQFP144	plastic thermal enhanced low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm; exposed die pad	SOT612-4
SAF3560HV/V1102	HLQFP144	plastic thermal enhanced low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm; exposed die pad	SOT612-4
SAF3560HV/V1103	HLQFP144	plastic thermal enhanced low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm; exposed die pad	SOT612-4

Table 3. Main applications

Type number	Main application	Option
SAF3560HV/V1100	HD Radio 1.0	single tuner
SAF3560HV/V1101	HD Radio 1.0 + Conditional Access (CA)	single tuner
SAF3560HV/V1102	HD Radio 1.5	dual tuner
SAF3560HV/V1103	HD Radio 1.5 + Conditional Access (CA)	dual tuner

5. Block diagram

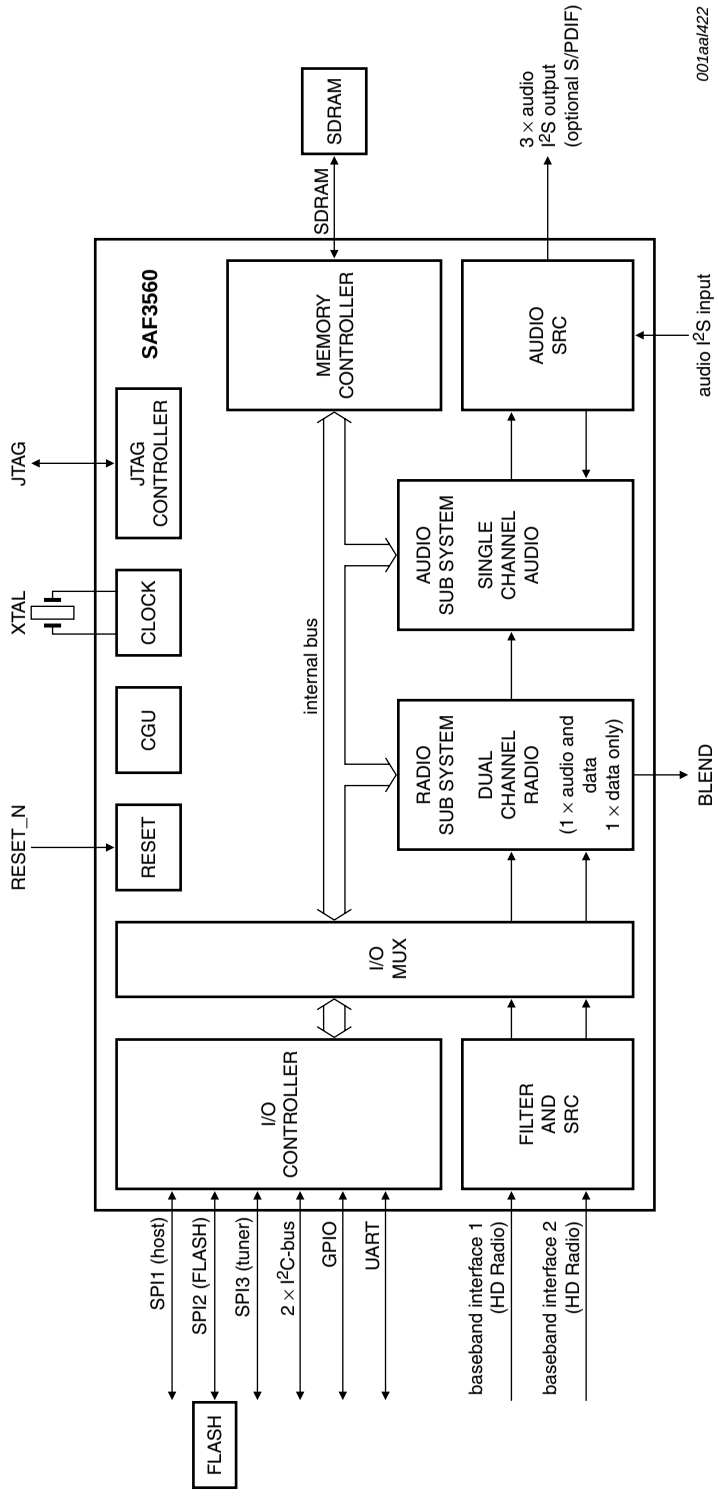


Fig 2. Block diagram of SAF3560

6. Pinning information

6.1 Pinning

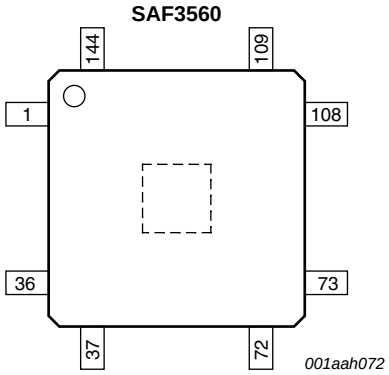


Fig 3. Pin configuration (HLQFP144)

Table 4. Pin allocation table (HLQFP144)

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	CLKOUT	2	RESET_N	3	I2C1_SCL	4	I2C1_SDA
5	I2C1_DA	6	$V_{DDD(MC)(3V3)}$	7	I2C2_SCL	8	I2C2_SDA
9	I2C2_DA	10	SPI1_SO	11	SPI1_SI	12	SPI1_SCLK
13	SPI1_SS_N	14	$V_{DDD(C)(1V2)}$	15	$V_{DDD(MC)(3V3)}$	16	SPI2_MI
17	SPI2_MO	18	SPI2_SCLK	19	SPI2_SS1_N	20	SPI2_SS2_N
21	$V_{DDD(MC)(3V3)}$	22	SPI2_SS3_N	23	SPI2_SS4_N	24	UART_TD
25	UART_RD	26	UART_RTS	27	$V_{DDD(C)(1V2)}$	28	$V_{DDD(MC)(3V3)}$
29	UART_CTS	30	SPI3_MISO	31	SPI3_MOSI	32	SPI3_SCLK
33	SPI3_SS1_N	34	$V_{DDD(DAB)(3V3)}$	35	SPI3_SS2_N	36	GPIO0
37	GPIO1	38	GPIO2	39	GPIO3	40	GPIO4
41	-[1]	42	$V_{DDD(DAB)(3V3)}$	43	-	44	-
45	-	46	-	47	-	48	-
49	-	50	-	51	-	52	-
53	-	54	-	55	BB1_I2S_BCK	56	BB1_I2S_WS
57	BB1_I2S_I	58	BB1_I2S_Q	59	BB2_I2S_BCK	60	BB2_I2S_WS
61	BB2_I2S_I	62	BB2_I2S_Q	63	$V_{DDD(C)(1V2)}$	64	$V_{DDD(DSP)(3V3)}$
65	HBCKOUT	66	I2S1_O_BCK	67	I2S1_O_WS	68	I2S1_O_SD
69	BLEND	70	$V_{DDD(MEM)(1V2)}$	71	$V_{DDD(DSP)(3V3)}$	72	I2S2_O_SD
73	I2S3_O_SD/ SPDIF_O	74	I2S_I_WS	75	I2S_I_BCK	76	I2S_I_SD
77	SDRAM_DIO0	78	SDRAM_DIO1	79	SDRAM_DIO2	80	$V_{DDD(SDRAM)(3V3)}$
81	SDRAM_DIO3	82	SDRAM_DIO4	83	SDRAM_DIO5	84	SDRAM_DIO6
85	$V_{DDD(SDRAM)(3V3)}$	86	SDRAM_DIO7	87	SDRAM_DIO8	88	SDRAM_DIO9
89	SDRAM_DIO10	90	$V_{DDD(SDRAM)(3V3)}$	91	$V_{DDD(C)(1V2)}$	92	SDRAM_DIO11

Table 4. Pin allocation table (HLQFP144) *...continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
93	SDRAM_DIO12	94	SDRAM_DIO13	95	SDRAM_DIO14	96	$V_{DDD(SDRAM)(3V3)}$
97	SDRAM_DIO15	98	SDRAM_WE_N	99	SDRAM_DQM0	100	SDRAM_DQM1
101	$V_{DDD(SDRAM)(3V3)}$	102	$V_{DDD(MEM)(1V2)}$	103	SDRAM_BA0	104	SDRAM_BA1
105	SDRAM_CS_N	106	SDRAM_RAS_N	107	$V_{DDD(SDRAM)(3V3)}$	108	SDRAM_CAS_N
109	SDRAM_CLKE	110	SDRAM_AO0	111	SDRAM_AO1	112	$V_{DDD(SDRAM)(3V3)}$
113	SDRAM_AO2	114	SDRAM_AO3	115	SDRAM_AO4	116	$V_{DDD(SDRAM)(3V3)}$
117	SDRAM_AO5	118	SDRAM_AO6	119	SDRAM_AO7	120	SDRAM_AO8
121	SDRAM_AO9	122	$V_{DDD(SDRAM)(3V3)}$	123	SDRAM_AO10	124	$V_{DDD(C)(1V2)}$
125	SDRAM_AO11	126	SDRAM_AO12	127	SDRAM_CLK	128	SDRAM_CLKIN
129	$V_{DDD(SDRAM)(3V3)}$	130	V_{SS}[2]	131	TRST_N	132	TCK
133	TMS	134	$V_{DDD(C)(1V2)}$	135	TDI	136	TDO
137	V_{SS}[2]	138	$V_{DDD(JTAG)(3V3)}$	139	$V_{DDA(PLL)(1V2)}$	140	$V_{DDA(OSC)(1V2)}$
141	XTALI	142	XTALO	143	$V_{DDD(MEM)(1V2)}$	144	V_{SS}[2]

[1] See Table 14 for unused pins.

[2] Global V_{SS} pin at backside contact

6.2 Pin description

Table 5. Pin description overview

Pin category	Details	Table number
Power supply pins	analog and digital supply pins	Table 6
Baseband interface pins	baseband and audio pins (I^2S-bus)	Table 7
Generic interface pins	GPIO and SPI3 pins	Table 8
SDRAM interface pins	data, address and control pins	Table 9
Serial NOR-Flash interface pins	SPI2 pins	Table 10
External host microcontroller interface pins	SPI1, I2C1, I2C2, UART, CLKOUT and RESET_N pins	Table 11
JTAG interface pins	JTAG pins	Table 12
Crystal oscillator pins	XTALI and XTALO pins	Table 13

Table 6. Pin description (power supplies)

Symbol	Pin	Type[1]	Description
Global ground supply			
V_{SS}	130, 137, 144 and backside contact	G	analog and digital global ground supply
Analog supplies			
$V_{DDA(OSC)(1V2)}$	140	P	oscillator analog supply voltage (1.2 V)
$V_{DDA(PLL)(1V2)}$	139	P	PLL analog supply voltage (1.2 V)
Digital supplies			
$V_{DDD(C)(1V2)}$	14, 27, 63, 91, 124 and 134	P	core digital supply voltage (1.2 V)
$V_{DDD(DAB)(3V3)}$	34 and 42	P	DAB digital supply voltage (3.3 V)

Table 6. Pin description (power supplies) *...continued*

Symbol	Pin	Type[1]	Description
$V_{DDD(DSP)(3V3)}$	64 and 71	P	DSP digital supply voltage (3.3 V)
$V_{DDD(JTAG)(3V3)}$	138	P	JTAG digital supply voltage (3.3 V)
$V_{DDD(MC)(3V3)}$	6, 15, 21 and 28	P	microcontroller digital supply voltage (3.3 V)
$V_{DDD(SDRAM)(3V3)}$	80, 85, 90, 96, 101, 107, 112, 116, 122 and 129	P	SDRAM digital supply voltage (3.3 V)
$V_{DDD(MEM)(1V2)}$	70, 102 and 143	P	memory digital supply voltage (1.2 V)

[1] Table 15 defines the pin type.

Table 7. Pin description (baseband interface)

Symbol	Pin	Type[1]	Description
Baseband interface			
BB1_I2S_BCK	55	IOZU-H	bit clock input and output of first baseband interface
BB1_I2S_I	57	IZU-H	I data input line of first baseband interface
BB1_I2S_Q	58	IZU-H	Q data input line of first baseband interface
BB1_I2S_WS	56	IOZU-H	word select input and output line of first baseband interface
BLEND	69	OL	blend indicator output, HIGH = digital audio / LOW = analog radio[2]
BB2_I2S_BCK	59	IOZU-H	bit clock input and output of second baseband interface
BB2_I2S_I	61	IZU-H	I data input line of second baseband interface
BB2_I2S_Q	62	IZU-H	Q data input line of second baseband interface
BB2_I2S_WS	60	IOZU-H	word select input and output line of second baseband interface
Audio interface			
HBCKOUT	65	IOZU	high-speed bit clock output[3]
I2S_I_BCK	75	IOZU-H	bit clock input and output line of I^2S-bus input interface
I2S_I_SD	76	IZU-H	serial data input line of I^2S-bus input interface
I2S_I_WS	74	IOZU-H	word select input and output line of I^2S-bus input interface
I2S3_O_SD/ SPDIF_O	73	OL	serial data output line of third I^2S-bus output interface; in alternative Sony/Philips digital output interface
I2S2_O_SD	72	OL	serial data output line of second I^2S-bus output interface
I2S1_O_BCK	66	IOZU-H	bit clock input and output line of first I^2S-bus output interface
I2S1_O_SD	68	OL	serial data output line of first I^2S-bus output interface
I2S1_O_WS	67	IOZU-H	word select input and output line of first I^2S-bus output interface

[1] Table 15 defines the pin type.

[2] Required for seamless switching between digital and analog AM/FM modes in HD Radio applications under bad reception conditions.

[3] $256 \times f_S$ output, required by some external DACs.

Table 8. Pin description (generic tuner interface)

Symbol	Pin	Type[1]	Description
GPIO interface			
GPIO4	40	IOZU	general purpose input and output port 4
GPIO3	39	IOZU	general purpose input and output port 3
GPIO2	38	IOZU	general purpose input and output port 2
GPIO1	37	IOZU	general purpose input and output port 1
GPIO0	36	IOZU	general purpose input and output port 0
SPI3 interface			
SPI3_MISO	30	IOZU-H	master input, slave output of third SPI interface
SPI3_MOSI	31	IOZU-H	master output, slave input of third SPI interface
SPI3_SCLK	32	IOZU-H	serial clock input and output of third SPI interface
SPI3_SS1_N	33	IOZU-H	slave select 1 input and output of third SPI interface (active LOW)
SPI3_SS2_N	35	OZU	slave select 2 output of third SPI interface (active LOW)

[1] Table 15 defines the pin type.

Table 9. Pin description (SDRAM interface)

Symbol	Pin	Type[1]	Description
Data input and output interface			
SDRAM_DIO15	97	IOL	data input and output bit 15
SDRAM_DIO14	95	IOL	data input and output bit 14
SDRAM_DIO13	94	IOL	data input and output bit 13
SDRAM_DIO12	93	IOL	data input and output bit 12
SDRAM_DIO11	92	IOL	data input and output bit 11
SDRAM_DIO10	89	IOL	data input and output bit 10
SDRAM_DIO9	88	IOL	data input and output bit 9
SDRAM_DIO8	87	IOL	data input and output bit 8
SDRAM_DIO7	86	IOL	data input and output bit 7
SDRAM_DIO6	84	IOL	data input and output bit 6
SDRAM_DIO5	83	IOL	data input and output bit 5
SDRAM_DIO4	82	IOL	data input and output bit 4
SDRAM_DIO3	81	IOL	data input and output bit 3
SDRAM_DIO2	79	IOL	data input and output bit 2
SDRAM_DIO1	78	IOL	data input and output bit 1
SDRAM_DIO0	77	IOL	data input and output bit 0
Address output interface			
SDRAM_AO12	126	OZU	address output bit 12
SDRAM_AO11	125	OZU	address output bit 11
SDRAM_AO10	123	OZU	address output bit 10
SDRAM_AO9	121	OZU	address output bit 9
SDRAM_AO8	120	OZU	address output bit 8
SDRAM_AO7	119	OZU	address output bit 7
SDRAM_AO6	118	OZU	address output bit 6

Table 9. Pin description (SDRAM interface) *...continued*

Symbol	Pin	Type[1]	Description
SDRAM_AO5	117	OZU	address output bit 5
SDRAM_AO4	115	OZU	address output bit 4
SDRAM_AO3	114	OZU	address output bit 3
SDRAM_AO2	113	OZU	address output bit 2
SDRAM_AO1	111	OZU	address output bit 1
SDRAM_AO0	110	OZU	address output bit 0
Control interface			
SDRAM_BA1	104	OZU	bit 1 of bank address output
SDRAM_BA0	103	OZU	bit 0 of bank address output
SDRAM_CAS_N	108	OZU	column address selector output (active LOW)
SDRAM_CLK	127	OZU	clock output
SDRAM_CLKE	109	OZU	clock enable output
SDRAM_CLKIN	128	IZU	clock input for re-synchronization
SDRAM_CS_N	105	OZU	chip select output (active LOW)
SDRAM_DQM1	100	OL	MSByte of data qualifier mask output
SDRAM_DQM0	99	OL	LSByte of data qualifier mask output
SDRAM_RAS_N	106	OZU	row address selector output (active LOW)
SDRAM_WE_N	98	OZU	write enable output (active LOW)

[1] Table 15 defines the pin type.

Table 10. Pin description (serial NOR-Flash interface)

Symbol	Pin	Type[1]	Description
SPI2 interface			
SPI2_MI	16	IZU	master input of second SPI interface
SPI2_MO	17	OZD	master output of second SPI interface
SPI2_SCLK	18	OZU	serial clock output of second SPI interface
SPI2_SS1_N	19	OZU	slave select 1 output of second SPI interface (active LOW)
SPI2_SS2_N	20	OZU	slave select 2 output of second SPI interface (active LOW)
SPI2_SS3_N	22	OZU	slave select 3 output of second SPI interface (active LOW)
SPI2_SS4_N	23	OZU	slave select 4 output of second SPI interface (active LOW)

[1] Table 15 defines the pin type.

Table 11. Pin description (external host microcontroller interface)

Symbol	Pin	Type[1]	Description
CLKOUT	1	OL	clock output; clock source and clock frequency are programmable through software
RESET_N	2	IZU-H	master reset input from host microcontroller (active LOW)
I²C-bus interface (master and slave)			
I2C2_DA	9	IOZD-H	data acknowledge input and output of the I²C-bus interface 2
I2C2_SCL	7	IOZU	serial clock input and output of the I²C-bus interface 2
I2C2_SDA	8	IOZU	serial data input and output of the I²C-bus interface 2
I2C1_DA	5	IOZD-H	data acknowledge input and output of the I²C-bus interface 1
I2C1_SCL	3	IOZU	serial clock input and output of the I²C-bus interface 1
I2C1_SDA	4	IOZU-H	serial data input and output of the I²C-bus interface 1
SPI1 interface			
SPI1_SCLK	12	IZU-H	serial clock input of first SPI interface
SPI1_SI	11	IZU-H	slave input of first SPI interface
SPI1_SO	10	OL	slave output of first SPI interface
SPI1_SS_N	13	IZU-H	slave select input of first SPI interface (active LOW)
UART interface			
UART_CTS	29	IZU	UART clear-to-send signal input
UART_RD	25	IZU	UART receive data input
UART_RTS	26	OH	UART ready-to-send signal output
UART_TD	24	OH	UART transmit data output

[1] Table 15 defines the pin type.

Table 12. Pin description (JTAG interface)

Symbol	Pin	Type[1]	Description
TCK	132	IZU	test clock input
TDI	135	IZU	test serial data input
TDO	136	OL	test serial data output
TMS	133	IZU	test mode select input
TRST_N	131	IZU	test reset input; drive LOW for normal operating

[1] Table 15 defines the pin type.

Table 13. Pin description (crystal oscillator)

Symbol	Pin	Type[1]	Description
XTALI	141	AI	crystal oscillator analog input
XTALO	142	AO	crystal oscillator analog output

[1] Table 15 defines the pin type.

Table 14. Pin description (internally connected pins)

Symbol	Pin	Type	Description
i.c.	41, 43 to 54	-	internally connected; leave open

Table 15. Pin type description

Type	Description	Unused pins[1]
Generic pin types		
AI	analog input pin	always connect to quartz crystal
AO	analog output pin	always connect to quartz crystal
G	ground pin	use all ground pins
IOL	digital input and output; drives LOW after reset	can be left open
IOZD	digital input and output pin with weak pull-down	can be left open
IOZU	digital input and output pin with weak pull-up	can be left open
IZU	digital input pin with weak pull-up	can be left open
OH	digital output; drives HIGH after reset	can be left open
OL	digital output; drives LOW after reset	can be left open
OZD	digital output pin with weak pull-down	can be left open
OZU	digital output pin with weak pull-up	can be left open
P	power supply pin	use all power supply pins
Specific pin types		
-H	pins with hysteresis	see generic types

[1] Applications, which do not need all pins from SAF3560, can treat unused pins as indicated without damage or malfunction of the device.

7. Limiting values

Table 16. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DDA(OSC)(1V2)}$	oscillator analog supply voltage (1.2 V)			−0.5	+1.7	V
$V_{DDA(PLL)(1V2)}$	PLL analog supply voltage (1.2 V)			−0.5	+1.7	V
$V_{DDD(C)(1V2)}$	core digital supply voltage (1.2 V)			−0.5	+1.7	V
$V_{DDD(DAB)(3V3)}$	DAB digital supply voltage (3.3 V)			−0.5	+3.9	V
$V_{DDD(DSP)(3V3)}$	DSP digital supply voltage (3.3 V)			−0.5	+3.9	V
$V_{DDD(JTAG)(3V3)}$	JTAG digital supply voltage (3.3 V)			−0.5	+3.9	V
$V_{DDD(MC)(3V3)}$	microcontroller digital supply voltage (3.3 V)			−0.5	+3.9	V
$V_{DDD(SDRAM)(3V3)}$	SDRAM digital supply voltage (3.3 V)			−0.5	+3.9	V
$V_{DDD(MEM)(1V2)}$	memory digital supply voltage (1.2 V)			−0.5	+1.7	V
T_{amb}	ambient temperature			−40	+85	°C
T_{stg}	storage temperature			−65	+150	°C
V_{ESD}	electrostatic discharge voltage	human body model	[1]	-	±2000	V
		charged device model	[2]			
		corner pins		-	±750	V
		other pins		-	±500	V
I_{lu}	latch-up current	all supply voltages below the maximum values listed in this table	[2]	−100	+100	mA

[1] Class 2 according to *JEDEC JESD22-A114*.

[2] According to *AEC-Q100-G*.

8. Thermal characteristics

The SAF3560 has no special thermal requirements. The backside contact is needed for electrical reasons. For soldering considerations, see Section 10.

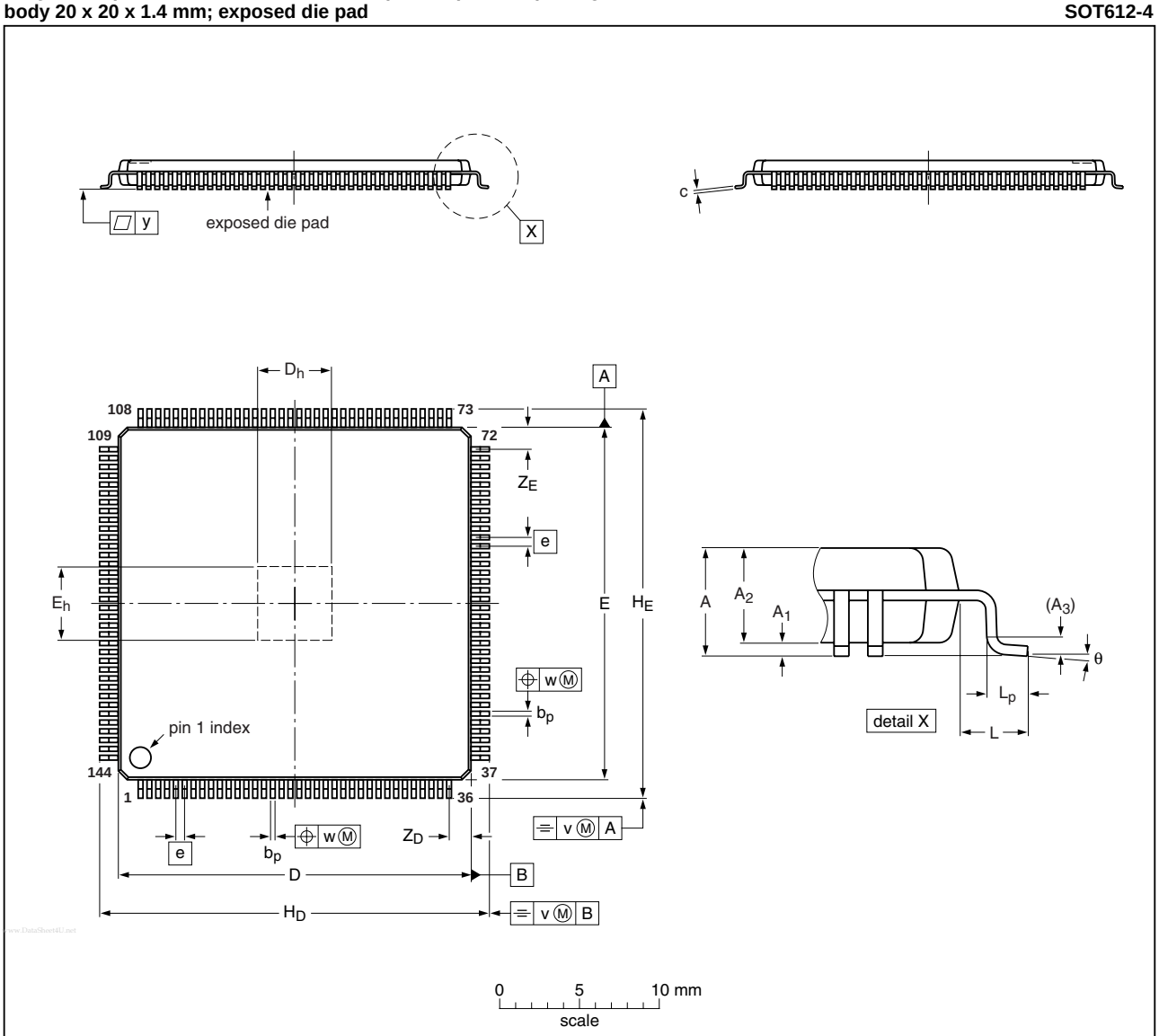
Table 17. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	26.3	K/W

[1] The overall $R_{th(j-a)}$ is based on JEDEC conditions and can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$ all power and ground pins must be connected to the power and ground layers directly. An ample amount of copper area directly under the SAF3560 with a number of through-hole plating, which connect to the ground layer (four-layer board: second layer), can also reduce the effective $R_{th(j-a)}$. Do not use any solder-stop varnish under the chip. In addition the use of soldering glue with a high thermal conductance after curing is recommended.

9. Package outline

HLQFP144: plastic thermal enhanced low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm; exposed die pad **SOT612-4**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.12 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	4.3 4.1	20.1 19.9	4.3 4.1	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7° 0°

Note

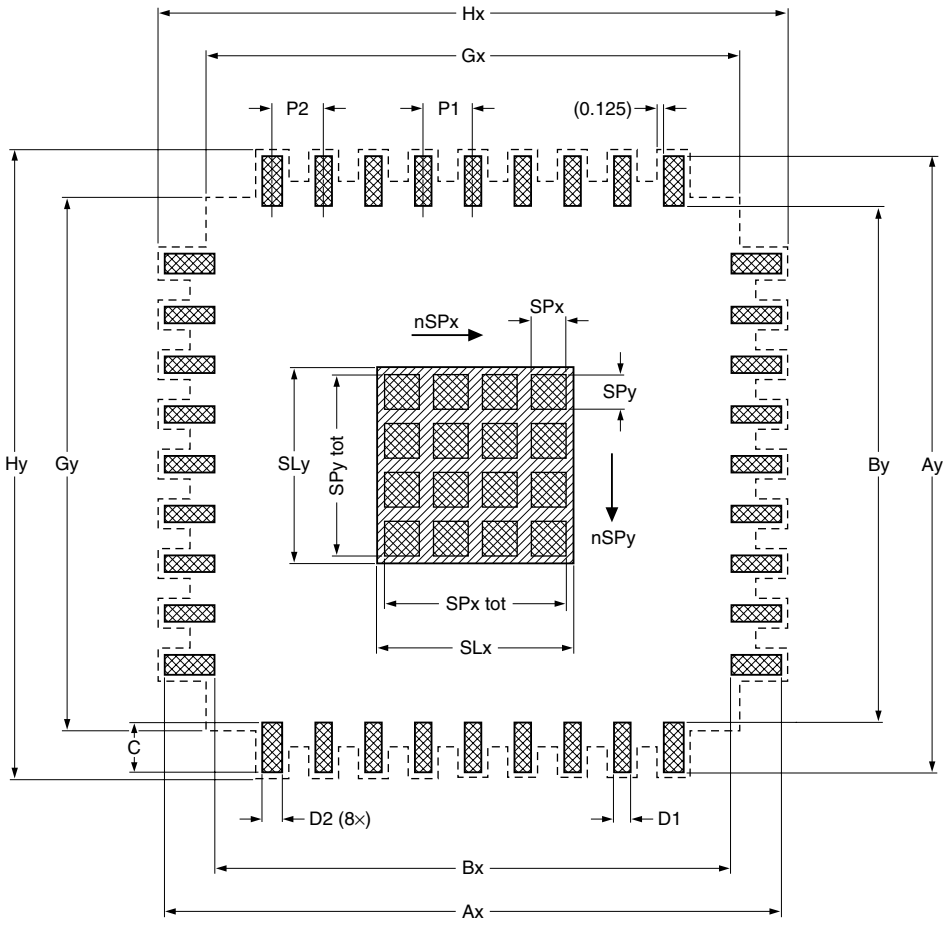
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT612-4		MS-026				~~07-12-11~~ 08-01-18

Fig 4. Package outline SOT612-4 (HLQFP144)

10. Soldering

Footprint information for reflow soldering of HLQFP144 package **SOT612-4**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

solder paste

occupied area

nSPx	nSPy
4	4

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy	SLx	SLy	SPx tot	SPy tot	SPx	SPy
0.500	0.560	23.300	23.300	20.300	20.300	1.500	0.280	0.400	20.500	20.500	23.550	23.550	4.500	4.500	4.400	4.400	0.750	0.750

Fig 5. Soldering footprint SOT612-4 (HLQFP144)

11. Abbreviations

Table 18. Abbreviations

Acronym	Description
AEC	Automotive Electronics Council
AM	Amplitude Modulation
BCK	Bit ClocK
CA	Conditional Access
CD	Compact Disc
CGU	Clock Generation Unit
CTS	Clear To Send
DAB	Digital Audio Broadcasting
DAC	Digital-to-Analog Converter
DSP	Digital Signal Processor
EPG	Electronic Program Guide
FM	Frequency Modulation
GPIO	General Purpose Input and Output
IF	Intermediate Frequency
I^2C-bus	Inter-IC bus
I^2S	Inter-IC Sound
I/O	Input/Output
JEDEC	Joint Electronic Device Engineering Council
JTAG	Joint Test Action Group
MUX	MUltipleXer
PLL	Phase-Locked Loop
RAM	Random Access Memory
RS232	Recommended Standard 232[1]
RTS	Ready To Send
SD	Secure Digital memory card
SDR	Single Data Rate
SDRAM	Synchronous Dynamic RAM
SPI	Serial Peripheral Interface
S/PDIF	Sony/Philips Digital InterFace
SRC	Sample-Rate Converter
UART	Universal Asynchronous Receiver Transmitter
WS	Word Select

[1] A serial interface.

12. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SAF3560_SDS v.3	20100915	Product short data sheet	-	SAF3560_SDS v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted where appropriate. • Minor text changes			
SAF3560_SDS v.2	20100503	Product short data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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15. Contents

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